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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,832	12/26/2001	Weiying Ding	015114-054300US	9038

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EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,832	DING ET AL.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15 and 19-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-14,16-18 and 23-30* is/are allowed.

6)☒ Claim(s) *19-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to the applicant's amendments

Applicants' argument with respect to the amended claims 19-22 filled on 07/21/05 have been fully considered but they are not persuasive. Applicants' argument with respect to the amended claims 1-18 and 25-30 filled on 07/21/05 have been fully considered and allowed.

RCE

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/21/05 has been entered.

Response to the applicant's argument

The applicant's argues that the prior art (Yin) fail to teach, "means for selecting using address bits". However, the argument is not convincing since Yin et al. teach or disclose a structure and a method for testing, programming and verification of a programming logic device (PLD) (see abstract). Further, Yin et al. in figure 1 and 2 teach a register group (50) includes first registers (row register) (53) and second registers (column register) (52) whereby the first and second registers coupled to a memory cell (20). Furthermore, Yi et al. teach means for selecting a location of memory cells to be programmed verified and tested in programmable logic device (see claim 24). As for selecting using address bits, the examiner disagrees and asserts that any register or storage in a memory system inherently comprises an address bits to select or identify locations in the memory system. In light of the above, the inclusion of the term "address bit" in

the claims does not change the concept of the claimed invention such that it is allowable over the prior art of record. Therefore, the applicants' argument although acknowledged, has not been found to be convincing.

Detailed Action

- Claims 23 and 24 have been previously allowed.
- Claims 19-22 remain pending and claims 1-18 and 25-30 are allowed.

Claim objections

1. Claim 15 objected to because of the following informalities:

Please define the full word of a written word or phrase for the **abbreviations** "ISC" as specified in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims **19-22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yin et al. (U.S. PN: 5,970,005)

As per claim **19:**

Yi et al. teach all the subject matter claimed in claim 1 including Yin et al. teach or disclose a structure and a method for testing, programming and verification of a programming logic device (PLD) (see abstract). Yin et al. that the PLD device comprises an array of programmable memory cells, arranged as rows and columns, to store the configuration information (see col. 2, last paragraph). Further, Yin et al. in figure 1 and 2 teach a register group (50) includes first registers (row register) (53) and second registers (column register) (52) whereby the first and second registers coupled to a memory cell (20). Furthermore, Yi et al. teach means for selecting a location of memory cells to be programmed verified and tested in programmable logic device (see claim 24).

As per claim **20,** Yi et al. teach all the subject matter claimed in claim 19 including Yi et al. teach a programmable logic device comprising bit programming for programming PLD device bit by bit and bit verification for verifying the PLD bit by bit (see claim 16).

As per claims **21 and 22,** Yi et al. teach all the subject matter claimed in claim 19 including Yi et al. teach a programmable logic device shifting column address to a column address register to select the column containing the cells to be programmed and shifting in a row data to a row data shift register to select the rows to be programmed (see claim 19).

Examiner's statement for reason for allowance

3. Claims **1-18 and 25-30** have been allowed.

Claims 23 and 24 have been previously allowed.

The following is an examiner's statement for allowance:

As per claim 1:

The prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious loading second data bits from first memory cells into the first registers, the first memory cells being in a first word line selected by first address bits in second registers; selecting, by a selection circuit responsive to the first address bits, a second word line; loading the first data bits into second memory cells, the second memory cells being the word line. Consequently, claim 1 is allowed over the prior art.

Claims **2-9,** which is/are directly or indirectly dependent/s of claim 1 is also allowable over the prior art of record.

As per claim 10:

The prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious first registers, each of the first registers being coupled to one of the rows of memory cells through interconnection conductors, first address bits being stored in the first registers; and second registers, each of the second registers being coupled to one of the columns of memory cells through interconnection conductors, first data bits stored in a first row of the memory cells being loaded into the second registers when the first row is selected by the fires address bits via a selection circuit, and second data bits stored in the second registers being programmed into a second row of the memory cells when the second row is selected by the first address bits via the selection circuit. Consequently, claim 10 is allowed over the prior art.

Claims **11-14 and 16-18,** which is/are directly or indirectly dependent/s of claim 10 is also allowable over the prior art of record.

As per claim 25:

The prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious loading second data bits from first memory cells in a first word line into the first registers, the first memory cells being selected by a selection operation using first address bits; selecting a second word line using a second selection operation using the first address bits; loading the first data bits into second memory cells in the second word line; shifting third data bits into the first registers while shifting the second data bits out of the registers; and loading the third data bits into third memory cells in a third word line. Consequently, claim 25 is allowed over the prior art.

Claims **26-28,** which is/are directly or indirectly dependent/s of claim 25 is also allowable over the prior art of record.

As per claim 29:

The prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a first plurality of registers, each of the registers being coupled to one of the columns of memory cells through interconnection conductors, wherein first data bits stored in a first row of the memory cells are loaded into the first registers; wherein the memory cells are in first word line selected by a selection circuit responsive to first address bits; and a first plurality of latches, each of the latches being coupled to one of first plurality of registers, wherein the first data bits are shifted out of the first registers while second data bits are shifted into the first registers, the second data bits being stored in the first plurality of latches and programmed into a second row

of the memory cells; wherein the second word of memory cells are in a second word line selected by the selection circuit responsive to the first address bit. Consequently, claim 29 is allowed over the prior art.

Claim **30,** which is/are directly or indirectly dependent/s of claim 29 is also allowable over the prior art of record.

4. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300.

Conclusion

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Esaw Abraham

Art unit: 2133

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